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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): Zhijian Xie et al.
Case: 3-4
Serial No.: 10/623,983
Filing Date: July 21, 2003
Group: 2826
Examiner: Fetsum Abraham

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450.

Signature: _____ Date: May 18, 2006

Title: Shielding Structure for Use in a Metal-Oxide-Semiconductor Device

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APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Sir:

Applicants (hereinafter referred to as "Appellants") hereby appeal the final rejection of claims 1-11 and 13-17 of the above-referenced application.

REAL PARTY IN INTEREST

The present application is assigned to Agere Systems Inc., as evidenced by an assignment recorded July 21, 2003 in the U.S. Patent and Trademark Office at Reel 014318, Frame 0159. The assignee, Agere Systems Inc., is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and interferences.

STATUS OF CLAIMS

Claims 1-18 are pending in the present application. Claims 12 and 18 have been objected to, but have been indicated as being allowable. Claims 1-11 and 13-17 stand finally rejected under one or more of 35 U.S.C. §112, second paragraph, 35 U.S.C. §102(b) and 35 U.S.C. §103(a). Claims 1-11 and 13-17 are appealed.

STATUS OF AMENDMENTS

An Amendment After Final Rejection Under 37 C.F.R. §1.116 was filed by Appellants on February 17, 2006. In this amendment, claims 12 and 18, which were indicated as containing allowable subject matter, were rewritten into independent form including all of the limitations of their respective base claims and any intervening claims, and claim 9 was canceled without prejudice. In an Advisory Action (Form PTOL-303) dated March 14, 2006, the Examiner indicated that the amendments after final rejection would not be entered. Appellants respectfully submit that these amendments after final rejection should have been entered by the Examiner because claims 12 and 18 would be presented in a form indicated as allowable and they clearly place the application in better form for appeal by materially reducing or simplifying the issues for appeal and would not require further consideration and/or search. The cancellation of claim 9, for example, would render moot the §112 rejection in the present application.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates generally to semiconductor devices, and more particularly to techniques for improving high-frequency performance in a metal-oxide-semiconductor (MOS) device (Specification; page 1, lines 4-6).

Embodiments of the invention provide techniques for improving high-frequency performance of a MOS device without significantly impacting hot carrier injection (HCI) degradation characteristics of the device (Specification; page 2, lines 11-12). The techniques of the invention can be used to fabricate an integrated circuit device, such as, for example, a laterally diffused MOS device, using conventional complementary MOS (CMOS) compatible process technology, and

therefore the cost of fabricating such a device is not significantly increased (Specification; page 2, lines 13-15).

In an illustrative embodiment of the invention, as depicted in FIG. 2 of the drawings, an exemplary laterally diffused MOS (LDMOS) device includes a source region 210 and a drain region 212 formed in an epitaxial layer 202 of a wafer 200 (Specification; page 5, lines 22-23). The source and drain regions 210, 212 have a conductivity type associated therewith which is opposite a conductivity type of a substrate 201, so that active regions can be formed in the device (Specification; page 5, lines 26-28). A channel region 216 and a drift region, which may comprise a first lightly doped drain (LDD) region (ldd1) 218 and a second LDD region (ldd2) 214, are formed in the LDMOS device (Specification; page 6, lines 14-15). The channel region 216 is formed near the source region 210 while the drift region extends from the channel region 216 to the drain region 212 (Specification; page 6, lines 15-17).

The exemplary LDMOS device further includes a gate 220 formed above at least a portion of the channel region 216 and proximate an upper surface of the wafer 200 (Specification; page 6, lines 22-23). A shielding electrode 222, which is referred to throughout the specification as a dummy gate, is formed in the LDMOS device between the gate 220 and the drain region 212 (Specification; page 6, lines 25-27). The dummy gate 222 is spaced laterally from the gate 220 and non-overlapping relative to the gate (Specification; page 6, lines 227-28). The dummy gate 222, which may be formed in virtually any configuration and/or shape that is non-overlapping with respect to the gate 220, reduces the Miller capacitance Cgd between the gate and drain of the LDMOS device, thereby improving the high-frequency performance of the device and reducing HCI degradation in the device (Specification; page 6, line 28, to page 7, line 5). The dummy gate 222 in the LDMOS device is electrically connected to the source region 210 using, for example, a conductive trace 232, contact vias 234 and a conductive plug 236 (Specification; page 7, lines 25-27).

FIGS. 3A-3I are cross-sectional views depicting illustrative steps in a semiconductor fabrication process which may be used in forming the exemplary LDMOS device shown in FIG. 2.

Independent claim 1 specifies a MOS device including a semiconductor layer of a first conductivity type, a first source/drain region of a second conductivity type formed in the semiconductor layer, and a second source/drain region of the second conductivity type formed in the semiconductor layer and spaced apart from the first source/drain region. The MOS device further includes a gate formed proximate an upper surface of the semiconductor layer and at least partially between the first and second source/drain regions, and a shielding structure formed proximate the upper surface of the semiconductor layer and between the gate and the second source/drain region. The shielding structure is electrically connected to the first source/drain region by way of a connection comprising a substantially vertical conductor formed in a region of the device overlying an active area of the device between the gate and the second source/drain region. The shielding structure is spaced laterally from the gate and is non-overlapping relative to the gate.

Independent claim 14 specifies an integrated circuit including at least one MOS device, the MOS device comprising a semiconductor layer of a first conductivity type, a first source/drain region of a second conductivity type formed in the semiconductor layer, and a second source/drain region of the second conductivity type formed in the semiconductor layer and spaced apart from the first source/drain region. The MOS device further includes a gate formed proximate an upper surface of the semiconductor layer and at least partially between the first and second source/drain regions, and a shielding structure formed proximate the upper surface of the semiconductor layer and between the gate and the second source/drain region. The shielding structure is electrically connected to the first source/drain region by way of a connection comprising a substantially vertical conductor formed in a region of the device overlying an active area of the device between the gate and the second source/drain region. The shielding structure is spaced laterally from the gate and is non-overlapping relative to the gate.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(I) Claim 9 stands rejected under 35 U.S.C. §112, second paragraph as being incomplete for omitting essential elements.

(II) Claims 1-3, 5-8 and 14-16 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,707,102 to Morikawa et al. (hereinafter "Morikawa").

(III) Claims 4, 10, 11, 13 and 17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Morikawa.

ARGUMENT

Appellants incorporate by reference herein the disclosures of all previous responses filed in the present application, namely, responses dated June 25, 2004, January 18, 2005, April 4, 2005 and February 17, 2006. Sections (I), (II) and (III) to follow will respectively address grounds (I), (II) and (III) presented above.

(I) With regard to the rejection of claim 9 under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, while Appellants do not necessarily agree that this claim omits essential elements, Appellants submit that the rejection is moot in view of the Amendment. The Examiner failed to enter the amendment, despite the fact that it clearly reduced the issues for appeal.

(II) With regard to the rejection of claims 1-3, 5-8 and 14-16 under 35 U.S.C. §102(b) as being anticipated by Morikawa, Appellants assert that Morikawa fails to provide the necessary disclosure necessary to sustain a §102(b) rejection.

It is well-established law that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Appellants assert that the rejection based on Morikawa does not meet this basic legal requirement. Support for this assertion follows.

Independent claims 1 and 14 recite a MOS device including a semiconductor layer of a first conductivity type, a first source/drain region of a second conductivity type formed in the semiconductor layer, and a second source/drain region of the second conductivity type formed in the semiconductor layer and spaced apart from the first source/drain region. The MOS device further includes a gate formed proximate an upper surface of the semiconductor layer and at least partially between the first and second source/drain regions, and a shielding structure formed proximate the upper surface of the semiconductor layer and between the gate and the second source/drain region. The shielding structure is electrically connected to the first source/drain region by way of a connection comprising a substantially vertical conductor formed in a region of the device overlying an active area of the device between the gate and the second source/drain region. The shielding structure is spaced laterally from the gate and is non-overlapping relative to the gate.

Morikawa, with reference to FIGS. 1 and 2, discloses a MOSFET device having a shield conductive film 10 formed above an n-type semiconductor region 8, between a gate electrode 3 and a drain 9 of the MOSFET device (Morikawa; column 5, lines 48-60). However, Morikawa fails to disclose, among other features of the claimed invention, a shielding structure electrically connected to the first source/drain region by way of a connection comprising a substantially vertical conductor formed in a region of the device overlying an active area of the device between the gate and the second source/drain region, as explicitly required by claims 1 and 14.

In the final Office Action, the Examiner contends that Morikawa, with reference to FIG. 2 thereof, teaches a power LDMOS device having a "shielding layer at least partially electrically connected to the first region (5) by way of [a] connection comprising [a] substantially vertical conductor formed in a region of the device overlying an active area (an area bounded between the source/drain regions 5 and 9)" (final Office Action; page 3, lines 9-13). Appellants strongly disagree. In providing support for the rejection, the Examiner refers to FIG. 2 of Morikawa showing an electrical connection between a shield conductive film 10, which the Examiner analogizes to the shielding structure set forth in claims 1 and 14, and wiring 13 which constitutes a source electrode. This connection, however, is not a physical connection but rather is a symbolic (schematic) representation of the actual physical connection between the source electrode wiring and the shield

conductive film. The Examiner's characterization of Morikawa is contrary to what is explicitly taught by Morikawa itself.

With reference to FIG. 1 and the text corresponding thereto, Morikawa clearly discloses that the actual physical connection between the source electrode wiring 13 and the shield conductive film 10 is made outside an active area of the device, and therefore such a connection arrangement is distinguishable from claims 1 and 14. In direct contrast to the claimed invention, Morikawa, with reference to FIG. 1 thereof, states that "wiring 13 is also electrically connected to the shield conductive film 10 via a contact hole 18, which is formed in the silicon oxide film 12 provided over the field oxide film 2 surrounding an active region L" (Morikawa; column 6, lines 10-14; FIG. 1; emphasis added). As is known by those having ordinary skill in the art, the field oxide film does not constitute an active area (e.g., a region in which active devices are formed) of an integrated circuit, but instead surrounds the active area. This is also clearly shown in FIG. 1 of Morikawa. In the claimed invention, unlike the connection arrangement taught by Morikawa, the connection itself between the shield structure and the first source/drain region, being formed in a region of the device overlying the active area, provides additional beneficial gate shielding so as to improve an effectiveness of the shielding structure over conventional methodologies.

Although a portion of the wiring 13 in the Morikawa device, which the Examiner analogizes to the "connection" set forth in claims 1 and 14, may traverse a region above an active area of the device (see FIG. 1 of Morikawa, which depicts a top plan view of the MOSFET device), Morikawa fails to explicitly disclose that the wiring 13 comprises "a substantially vertical conductor formed in a region of the device overlying an active area of the device between the gate and the second source/drain region," as required by claims 1 and 14 (emphasis added). Unlike the device configuration taught by Morikawa, because the connection between the shielding structure and the first source/drain region set forth in claims 1 and 14 comprises a substantially vertical conductor formed over the active area of the device, the connection itself provides additional beneficial gate shielding so as to improve an effectiveness of the shielding structure, without increasing a capacitance between the gate and the second source/region or between the gate and the first source/drain region. Since the electrical connection point between the shield conductive film 10 and

the wiring 13 in Morikawa is formed outside of the active region L of the device, the wiring provides essentially no additional shielding benefits to the device.

Appellants respectfully assert that claims 2, 3, 5-8, 15 and 16 are patentable over Morikawa not only due to their respective dependence from independent claims 1 and 14, but also because such claims respectively recite patentable subject matter in their own right. Accordingly, withdrawal of the §102(b) rejection of claims 1-3, 5-8 and 14-16 is respectfully requested.

(III) Regarding the §103(a) rejection of claims 4, 10, 11, 13 and 17 based on a modification of the teachings of Morikawa, Appellants submit that these claims are patentable over Morikawa due to their respective dependence from independent claims 1 and 14. Moreover, Appellants respectfully assert that the cited modification of Morikawa fails to establish a *prima facie* case of obviousness under 35 U.S.C. §103(a), as specified in M.P.E.P. §2143, and thus claims 4, 10, 11, 13 and 17 respectively recite patentable subject matter in their own right.

As set forth therein, M.P.E.P. §2143 states that three requirements must be met in order to establish a *prima facie* case of obviousness. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference, or references when combined, must teach or suggest all of the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must be found in the prior art, not in Appellants' disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). It is sufficient to show that a *prima facie* case of obviousness has not been established by showing that one of the requirements has not been met.

For example, claims 10 and 17 further define the shielding structure as being "formed relative to the gate such that a capacitance between the gate and the second source/drain region is minimized without substantially increasing a capacitance between the gate and the first source/drain region." Appellants submit that the cited modification of Morikawa fails to teach or suggest at least this additional feature.

> With regard to claims 10 and 17, the Examiner contends that:
>
> the insulation layers separating the shielding structures from the drain regions are thicker than the gate insulation layers used in the structures. Further, please note that the elevation of the shielding structures in relation to the position of the gate in vertical orientation is similar in both structures. Clearly, the lateral spacing difference between the gate and the shielding layer in both structures if there is one is immaterial so far as capacitance is concerned because the shielding layer is positioned on the drain region in both structures (final Office Action; page 5, first paragraph).

Appellants respectfully disagree with this contention. Claims 10 and 17 explicitly require that the shielding structure be formed in a specific manner which minimizes the capacitance between the gate and second source/drain region without substantially increasing the capacitance between the gate and first source/drain region. While the MOSFET device disclosed in Morikawa is intended to provide some reduction in gate-to-source capacitance (Cgs) and drain-to-source capacitance (Cds) compared to standard devices (Morikawa; column 10, lines 39-47), Morikawa fails to teach or suggest any arrangement of the shield conductive film which minimizes the capacitance between the gate and second source/drain region, without substantially increasing the capacitance between the gate and first source/drain region, as required by the subject claims. As stated in the present specification with reference to FIG. 2, the shielding structure (e.g., dummy gate 222) "is selectively located, in relation to the gate 220, so as to optimize an effectiveness of the dummy gate," which may be measured by "the amount of reduction in Miller capacitance Cgd and/or HCI degradation in the device" (Specification; page 7, lines 14-18).

For at least the reasons given above, Appellants respectfully request withdrawal of the §102(b) and §103(a) rejections of claims 1-8, 10, 11 and 13-17. Appellants believe that claims 1-3, 5-8 and 14-16 are not anticipated by Morikawa, and that claims 4, 10, 11, 13 and 17 are not obvious in view of Morikawa. As such, the application is asserted to be in condition for allowance, and favorable action is respectfully solicited.

Respectfully submitted,

Date: May 18, 2006

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CLAIMS APPENDIX

1. A metal-oxide-semiconductor (MOS) device, comprising:

a semiconductor layer of a first conductivity type;

a first source/drain region of a second conductivity type formed in the semiconductor layer;

a second source/drain region of the second conductivity type formed in the semiconductor layer and spaced apart from the first source/drain region;

a gate formed proximate an upper surface of the semiconductor layer and at least partially between the first and second source/drain regions; and

a shielding structure formed proximate the upper surface of the semiconductor layer and between the gate and the second source/drain region, the shielding structure being electrically connected to the first source/drain region by way of a connection comprising a substantially vertical conductor formed in a region of the device overlying an active area of the device between the gate and the second source/drain region, the shielding structure being spaced laterally from the gate and being non-overlapping relative to the gate.

2. The device of claim 1, wherein the shielding structure is connected to the first source/drain region by a conductive trace, the conductive trace being spaced substantially from the gate by an insulating layer formed between the gate and the conductive trace.

3. The device of claim 2, wherein the conductive trace is formed using a metalization process.

4. The device of claim 2, wherein the conductive trace is formed using at least a second level metalization process.

5. The device of claim 2, wherein the insulating layer comprises an oxide.

6. The device of claim 1, wherein the first source/drain region is a source of the device and the second source/drain region is a drain of the device.

7. The device of claim 1, wherein the device comprises a diffused MOS (DMOS) device.

8. The device of claim 1, wherein the device comprises a laterally diffused MOS (LDMOS) device.

9. The device of claim 1, wherein the device comprises a vertical diffused MOS device.

10. The device of claim 1, wherein the shielding structure is formed relative to the gate such that a capacitance between the gate and the second source/drain region is minimized without substantially increasing a capacitance between the gate and the first source/drain region.

11. The device of claim 1, wherein the shielding structure comprises at least one conductive plug.

13. The device of claim 1, further comprising an insulting layer formed on at least a portion of an upper surface of the device, the shielding structure comprising a conductive plug formed at least partially through the insulating layer.

14. An integrated circuit including at least one metal-oxide-semiconductor (MOS) device, the at least one MOS device comprising:

a semiconductor layer of a first conductivity type;

a first source/drain region of a second conductivity type formed in the semiconductor layer;

a second source/drain region of the second conductivity type formed in the semiconductor layer and spaced apart from the first source/drain region;

a gate formed proximate an upper surface of the semiconductor layer and at least partially between the first and second source/drain regions; and

a shielding structure formed proximate the upper surface of the semiconductor layer and between the gate and the second source/drain region, the shielding structure being electrically connected to the first source/drain region by way of a connection comprising a substantially vertical conductor formed in a region of the device overlying an active area of the device between the gate and the second source/drain region, the shielding structure being spaced laterally from the gate and being non-overlapping relative to the gate.

15. The integrated circuit of claim 14, wherein the shielding structure in the at least one MOS device is connected to the first source/drain region by a conductive trace, the conductive trace being spaced substantially from the gate by an insulating layer formed between the gate and the conductive trace.

16. The integrated circuit of claim 14, wherein the at least one MOS device comprises a laterally diffused MOS (LDMOS) device.

17. The integrated circuit of claim 14, wherein the shielding structure in the at least one MOS device is formed relative to the gate such that a capacitance between the gate and the second source/drain region is minimized without substantially increasing a capacitance between the gate and the first source/drain region.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.

Receipt in the USPTO is hereby acknowledged of:

Notice of Appeal - (Orig. & 1 copy)
Petition for Extension of Time Under
37 CFR 1.136(a) - (Orig. & 1 copy)

March 17, 2006
Xie 3-4
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